REMARKS

The Examiner has objected to the form of the Abstract. Accordingly, the present response amends the Abstract to conform to Patent Office requirements.

Claims 1-4 stand rejected under 35 U.S.C. 102(b) as being fully met by Patent 5,347,129-Miller et al. In applying Miller et al to the original claims, the Examiner states that measured data is digitalized by an analog-to-digital converter 16 so as to obtain digitalized measured data which is disseminated to a digital signal processor 20 for processing the digitalized measured data and outputting respective measured values. A shift register 18 of the FIFO type is positioned between the analog-to-digital converter and the digital signal processor for storing the digitalized measured data, and the shift register is read out to perform simultaneous computation by the processor.

By this response, independent claims 1 and 2 have been amended so as to patentably distinguish applicants' invention from Miller et al, as now will be explained.

The Miller et al measuring system serves different purposes and incorporates different functions when compared with the present invention. Miller et al's system is used for radiation detection and has dedicated features adapted for processing data representative of radiation values. For example, Miller et al disclose a single interface 18, having the capabilities of a pulse threshold trigger and a FIFO shift register, which collects a series of digitalized data points which have been sensed in analog form by a radiation detector 12, and passed through the analog-to-digital converter 16, in order to make preliminary calculations, including a cross correlation evaluation. By contrast, the present invention is intended to reduce the number of interrupts necessary to the

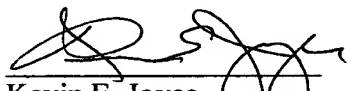
processing of collected data by a digital signal processor. To this end, measured analog data from multiple sensors are applied to a plurality of analog-to-digital converters arranged with a common output connection to which a shift register is joined, the shift register thereby collecting all digitalized measured data produced by the converters for subsequent application to a digital signal processor for simultaneous computation. A block transfer of all memory content in the shift register into the processor is effected whereby the number of computation steps is significantly reduced. As a result, all computation is done in the digital signal processor. As indicated above, with the Miller et al arrangement part of the computation, like cross correlation of measured data points, is effected in the interface 18, and only the remaining part of the computation is effected in the digital signal processor. Compared to the present invention, this leads to considerably slower processing of the measured data.

Claims 1 and 2 have been amended to recite that a plurality of analog-to-digital converters are provided with a common output connection which is joined to a shift register whereby digitalized measured data are intermediately stored until all digitalized measured data to be simultaneously computed by a digital signal processor is acquired by the register. By employing a plurality of analog-to-digital converters so joined to a shift register, it becomes possible to process more data simultaneously inasmuch as the shift registers are able to collect all data provided by the converters, and very fast process is obtained due to the fact that the data collected in the shift register can be block transferred to the digital signal processor without any computation being effected between the steps of analog-to-digital conversion and digital signal processing. By providing a plurality of analog-to-digital converters, and thus a plurality of measuring

instruments in parallel, it is possible to use measuring instruments of different types at the same time, e.g., voltage and current indicators used for calculating power consumption. The arrangement of a plurality of measuring instruments, each connected to a respective analog-to-digital converter having a common output connection joined to a shift register results in a reduction of the interrupts necessary to carry out the computation work in the digital signal processor, because a plurality of measurement data are obtained simultaneously, collected in the shift register and are applied in a block transfer to the digital signal processor for computation.

The method and apparatus now recited in amended main claims 1 and 2 are neither disclosed nor suggested by the Miller at al patent. Accordingly, applicants contend that the §102(b) rejection has been overcome, and that the application is in condition for allowance. Such action is therefore requested.

Respectfully submitted,



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